EXAMINER'S AMENDMENT

1. Claims 2-5, 7-9, 13-16, 18-21, 23-24, 26-28, 33, and 35-36 are allowed.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Nishitkumar V. Patel (Reg. No. 65,546) on 06/28/11.

The application has been amended as follows:

Replace **claim 23** with:

23. The computer system of claim 36, wherein said processor is configured ~~operable~~ to generate one of the test designs by identifying a plurality of inputs, wherein the plurality of inputs comprises the input pins of the ~~top level~~ module, one of the output lines of one of the parameterized submodules, and registers.

Replace **claim 24** with:

24. The computer system of claim 23, wherein said processor is configured ~~operable~~ to generate one of the test designs by identifying a plurality of outputs, wherein the outputs identified comprise the output pins of the ~~top level~~ module, one of the input lines of one of the parameterized submodules, and registers.

Replace **claim 33** with:

33. A method comprising:

Generating a plurality of test designs associated with a design automation tool, wherein the plurality of test designs comprises a module, wherein said generating the plurality of test designs comprises:

(a) instantiating an input/output (I/O) structure of the module having input and output pins;

(b) applying a function to select a plurality of submodules from a design module library, wherein the plurality of submodules comprises input and output lines, wherein the plurality of submodules is located within the module;

(c) parameterizing the plurality of submodules from the design module library for interconnection with the module;

(d) interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types, wherein the selection of the particular type of interconnect is based on a probabilistic function and wherein the plurality of interconnect types includes an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect; and

(~~c~~f) connecting the plurality of parameterized submodules to the input and output pins of the module.

Cancel **claim 34.**

Replace **claim 36** with:

36. A computer system comprising:

a memory configured ~~operable~~ to hold information associated with a design module library; and

a processor coupled to the memory, wherein said processor is configured ~~operable~~ to generate a plurality of test designs associated with a design automation tool, wherein the plurality of test designs comprises a ~~the~~ module, said processor is configured ~~operable~~ to:

(a) instantiate an input/output (I/O) structure of the module having input and output pins;

(b) apply a function to select a plurality of submodules from the design module library, wherein the plurality of submodules includes a plurality of input and output lines, wherein the plurality of submodules is located within the module;

(c) parameterize ~~parameterizing~~ the plurality of submodules from the design module library for interconnection with the module;

(d) interconnect the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types, wherein the selection of the particular type of interconnect is based on a probabilistic function and wherein the plurality of interconnect types includes an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect; and

(e) connect the plurality of parameterized submodules to the input and output pins of the module.

Cancel **claim 37**.

Replace **claim 39** with:

39. An apparatus comprising:

storage means for storing data design module library; and

processing means for generating a plurality of test designs associated with a design automation tool, wherein the plurality of test designs comprises a module, said processing means:

(a) for instantiating an input/output (I/O) structure of the module having input and output pins,

(b) for applying a function to select a plurality of submodules having input and output lines from the design module library, wherein the plurality of submodules is located within the module,

(c) for parameterizing the plurality of submodules from the design module library for interconnection with the module,

(d) for interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types, wherein the selection of the particular type of interconnect is based on a probabilistic function and wherein the plurality of interconnect types includes an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect; and

(e) for connecting the plurality of parameterized submodules to the input and output pins of the module.

Cancel **claim 41**.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance: claims 2-5, 7-9, 13-16, 18-21, 23-24, 26-28, 33, 35-36, 38-40, and 42 are considered allowable since when reading the claims in light of the specification, none of the references of record alone or in combination disclose or suggest the combination of limitations specified in the independent claims, specifically interconnecting the lines of the plurality of parameterized submodules in a test design for a programmable chip based on a selection of a particular type of interconnect from a plurality of interconnect types, wherein the selection of the particular type of interconnect is *based on a probabilistic function and wherein the plurality of interconnect types includes an interconnect having a mathematical expression, an interconnect having conditional logic, or a direct interconnect* as disclosed in independent claims 33, 36, and 39 of the instant application (as defined in specification Pg. 17 Lines 10-28 and Fig. 8).

Prior Art of Record

4. The Prior art of record **Chang et al.** (US Patent No. **6,269,467**) discloses (a) instantiating an input/output (I/O) structure of a module having input and output pins **(column 41, lines 4-11)**; (b) selecting a plurality of submodules, wherein the plurality of submodules comprises input and output lines **(column 8, lines 12-25)**; (c) parameterizing the plurality of submodules for interconnection with the module **(column 22, lines 53-59)**; (d) interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types **(column 23, lines 30-43)**; and (f) connecting the plurality of parameterize submodules to the input and output pins of the module **(column 24, lines 11-19)**.

Chang does not teach the limitations directed towards allowable subject matter as recited above.

The Prior art of record **Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow")** discloses selecting a plurality of submodules from a design module library **(page 51, column 2, 2nd paragraph)** wherein the said selecting the plurality of submodules is constrained based on a hardware family of the one of the test designs, wherein the hardware family is selected from a plurality of hardware families **(page 51, "Optimizing physical design", instantiating vendor-specific macro cells).**

Bening does not teach the limitations directed towards allowable subject matter as recited above.

The Prior art of record **Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1)** discloses teaches wherein instantiation constraints are used to select the plurality of submodules **([0085])**.

Zaidi does not teach the limitations directed towards allowable subject matter as recited above.

The Prior art of record **Dustin ("Automated Testing Tools")** discloses determining whether a predetermined number of test designs for testing the design automation tool has been generated **(page 4,**

1st paragraph); and applying the plurality of test designs to test the design automation tool **(page 4, 1st paragraph, help produce the integration test)**.

Dustin does not teach the limitations directed towards allowable subject matter as recited above.

The Prior art of record **Goossens ("Design of Heterogeneous ICs for Mobile and Personal Communication Systems")** discloses submodules comprising of adders and phase lock loops **(page 524-525, Figure 1, Section 3.2)**.

Goossens does not teach the limitations directed towards allowable subject matter as recited above.

The Prior art of record **Rajsuman** (US Patent No. **6,678,645**) discloses generating a plurality of test designs of an ASIC including DSP and memory submodules **(column 1, lines 16-29)**.

Rajsuman does not teach the limitations directed towards allowable subject matter as recited above.

Response to Arguments

5. The 35 U.S.C. 112 rejection has been withdrawn due to the amended claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUZANNE LO whose telephone number is (571)272-5876. The examiner can normally be reached on 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

/SL/
06/29/11